EDA: Electronic Design Automation

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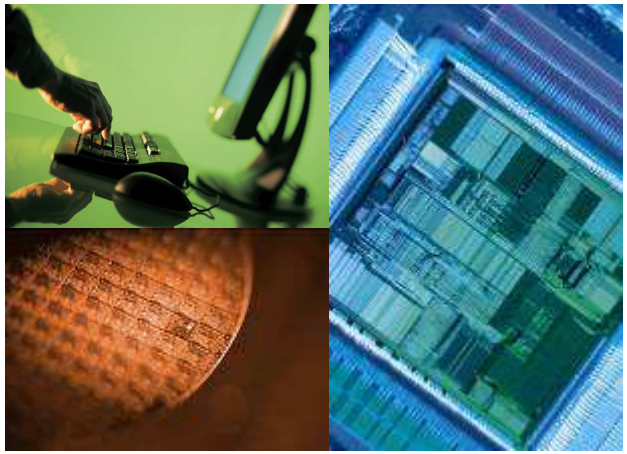

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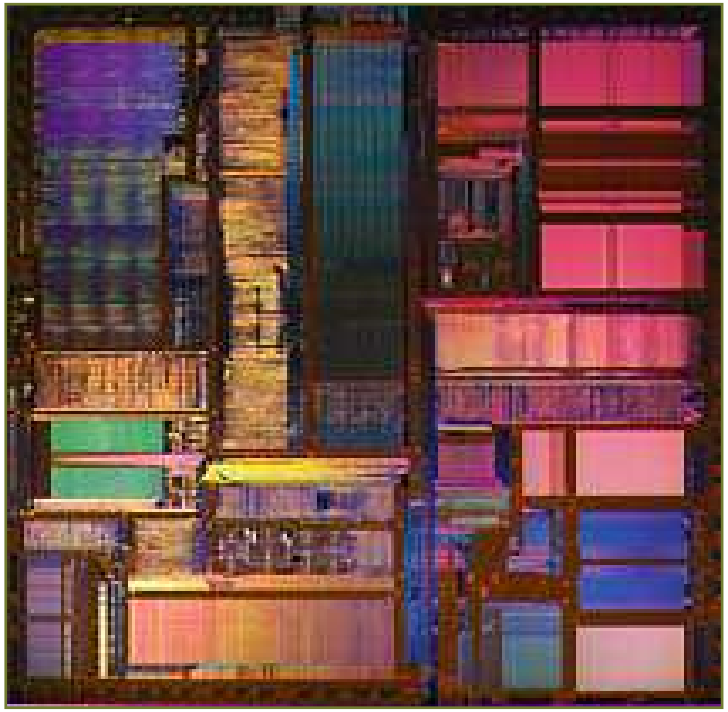
Contents

- What is EDA
- The Phases of IC design
- Opportunities for parallelism

Electronic Design Automation?

The software tools engineers use to design new ICs



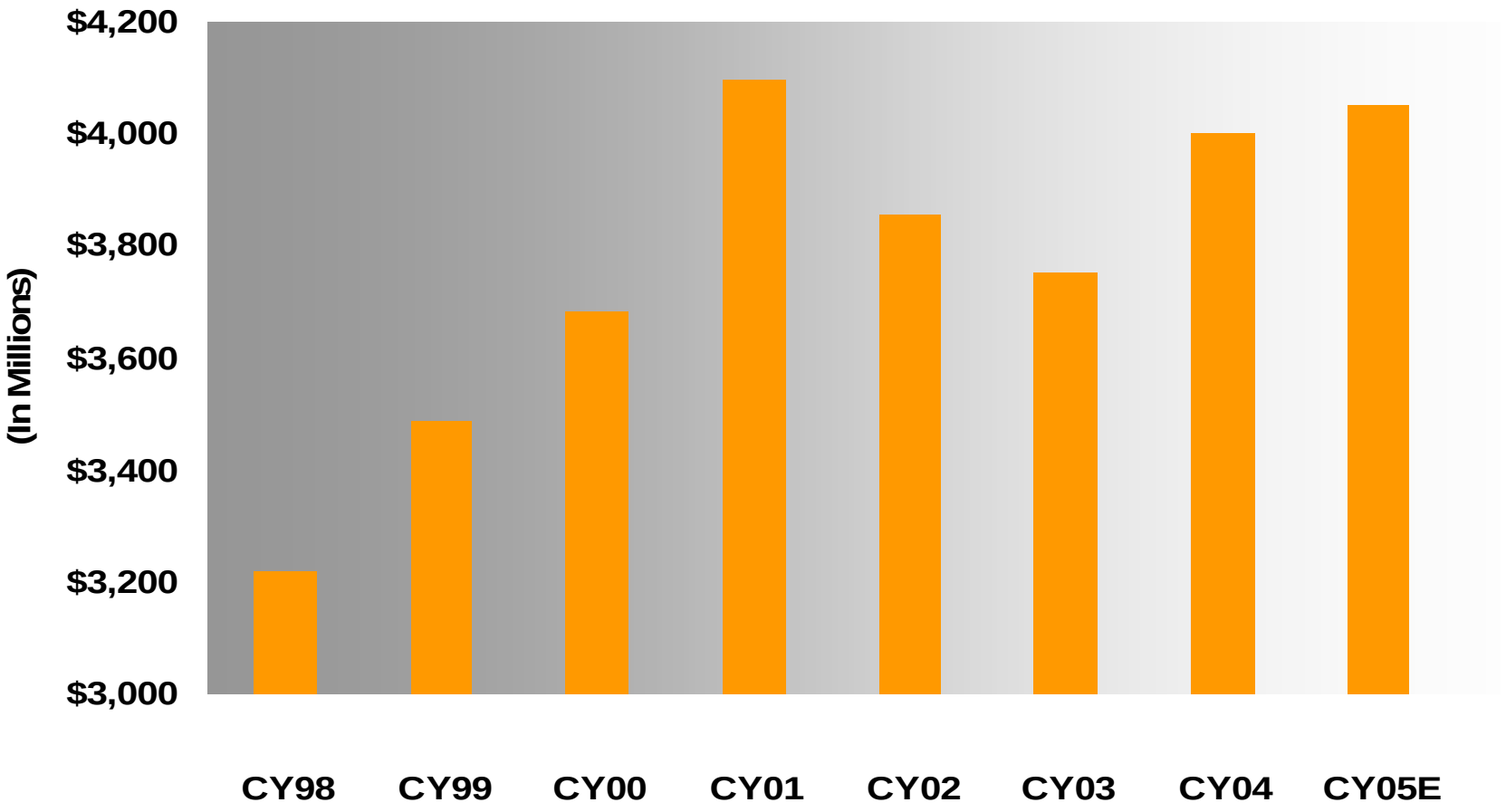
If Santiago were as crowded as this chip. . .

… the streets would be 8 cm. wide!

Main Applications

- Hardware Simulation
- Hardware Compilers
- Place & Route
- Formal Verification
- Mask generation
- Semiconductor Simulation
- etc.

The EDA Industry
(not including IP companies)



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The Cost of Staying in the Game

45 Nanometers Process, 300 Millimeters Wafers

Process Technology R&D	~$800M/year
Pilot Line	$1-2B
Wafer Fab	$3B
Design	$20-50M
Masks' Set (35-40 Masks)	~$8M
Test (SOC)	Up To 60¢/second

Source: A. Bryant, Intel 2005, IBS 2005, ITRS 2005

2005 Worldwide Top 10 Semiconductor Sales Leaders ($M)

2005 Rank	2004 Rank	Company	Headquarters	2004 ($M)	2005 ($M)	05/04 % Change
1	1	Intel	U.S.	$31,430	$35,395	13%
2	2	Samsung	South Korea	$15,830	$17,830	13%
3	3	TI	U.S.	$10,700	$11,300	6%
4	7	Toshiba	Japan	$8,589	$9,045	5%
5	6	ST	Europe	$8,756	$8,870	1%
6	4	Infineon	Europe	$9,180	$8,297	-10%
7	5	Renesas	Japan	$9,000	$8,266	-8%
8	8	TSMC*	Taiwan	$7,648	$8,217	7%
9	9	Sony	Japan	$5,070	$5,845	15%
10	10	Philips	Europe	$5,692	$5,646	-1%

*Foundry

Source: IC Insights, April 2006

Typical appliances

- Video decoders for DVD players and digital TV
- MP3 decoders/encoders
- Network routing
- Wifi adapters
- ICs for celular phones
- ICs for digital cameras
- etc.

EDA Players

- Cadence
- **Synopsys**
- Mentor
- Magma

- Software is very expensive
- Just a few customers
- Not robust

- Synopsys installed a R&D center in Chile in June 2006: first EDA R&D center in Latin-America
- 17 engineers and *growing*

Hardware Description Languages

- Verilog
- System Verilog
- VHDL

They were designed for simulation but they are used for synthesis now

Characteristics

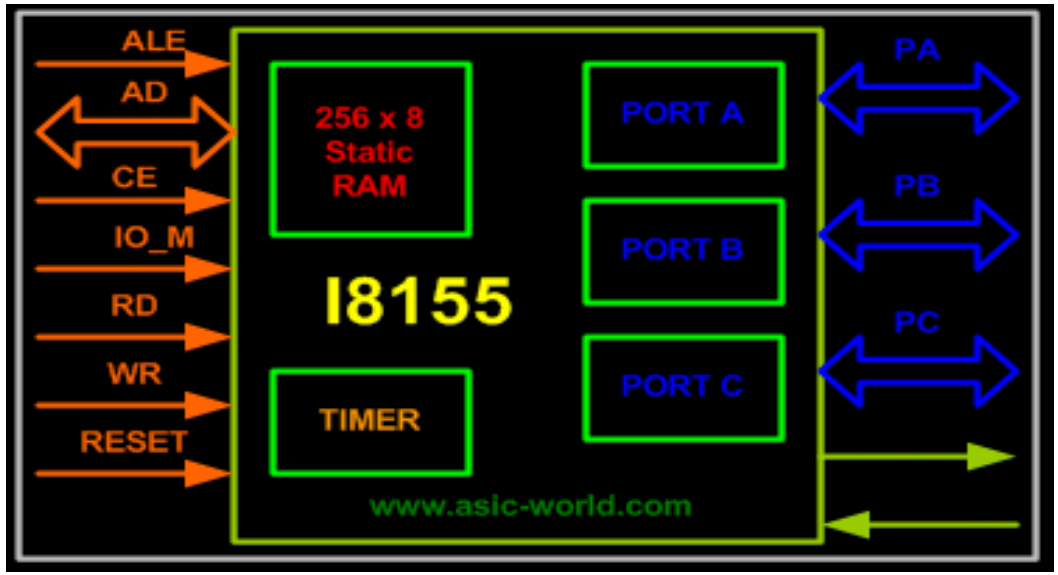
- Fully parallel
- Everytime you put a + you insert a hardware adder
- * is very expensive
- High level for simulation
- Low level for compiling: *not everything can be synthesized*
- No floating point
- You specify the width of every datum
- Different kinds of assignment

Phases of IC design

- Design
- RTL coding in Verilog
- Simulation
- Synthesis
- Formal Verification
- Place & Route
- Mask Generation
- Post Silicon Validation

Design

- What the IC is supposed to do
- Input and outputs

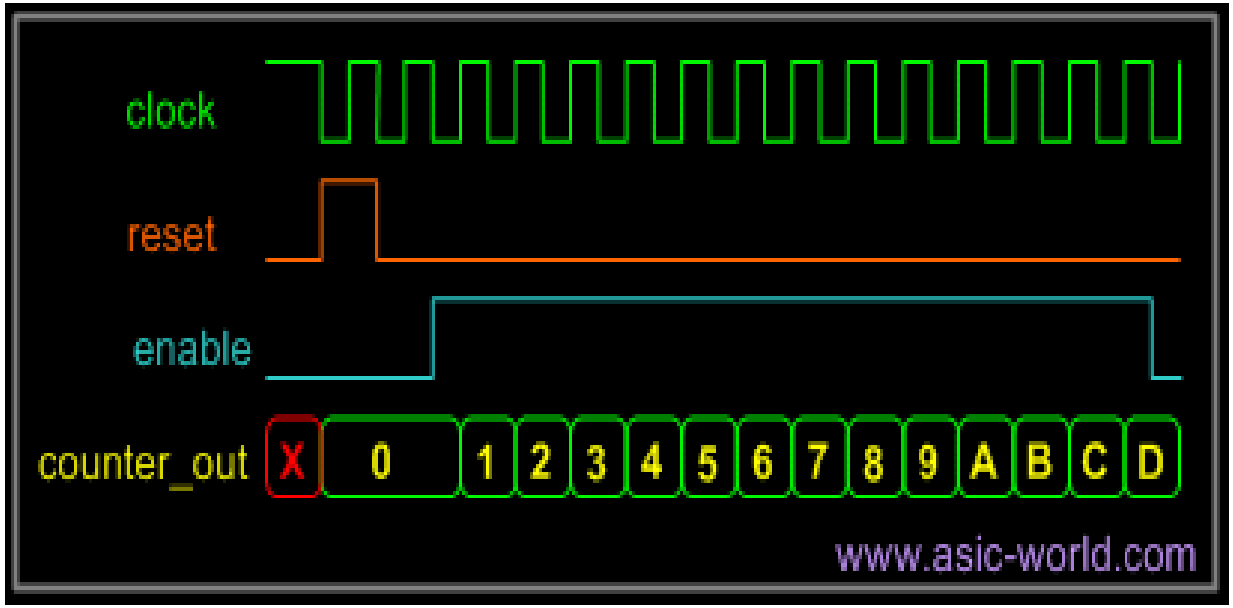


Implementation in an HDL: Coding in RTL

```
module counter ( input clock, input reset,
         input enable , output  [3:0] counter_out);
  wire clock, reset, enable;
  always @ (posedge clock) begin : COUNTER
    if (reset == 1'b1) begin
      counter_out <= 4'b0000;
    end
    else if (enable == 1'b1) begin
      counter_out <= counter_out + 1;
    end
  end
endmodule
```

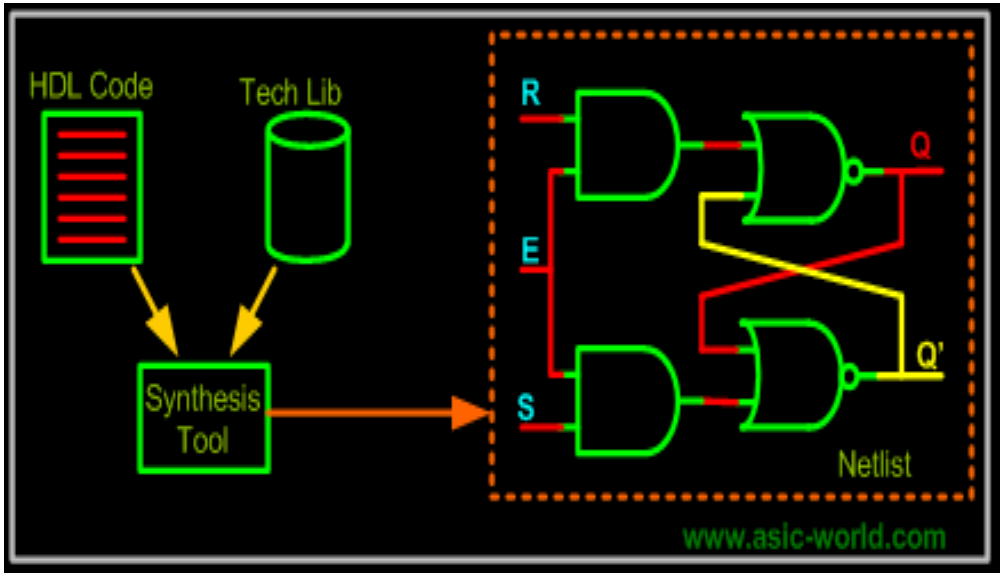
Simulation

- Use *timing diagrams*
- Give value to inputs
- Verify that the outputs are correct



Synthesis

- Translate the source program into a circuit
- Equivalent to compiling
- Very time consuming

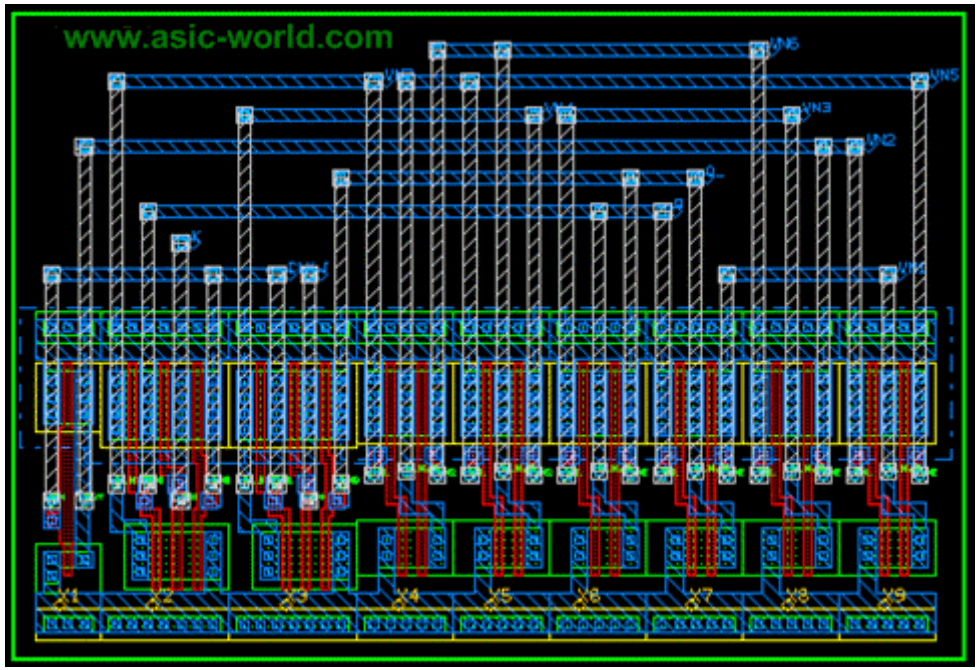


Formal Verification

- Proves that the output circuit of synthesis is a correct implementation of the source program
- Validates the output of the hardware compiler
- Very time consuming

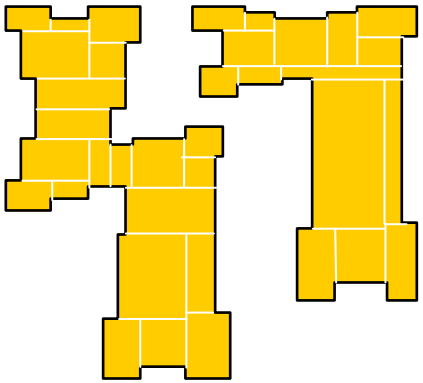
Place & Route

- Put gates and wires in the chip
- Very time consuming



Mask Generation

- Fracture polygons to trapezoids
- Make optical correction
- Write in a format readable for the fab
- Very time consuming



Post Silicon Validation

- put the IC in a real environment
- simulation is so slow that not everything is tested
- fully test the IC
- some bugs can still show

What the EDA customer wants

- Minimize IC area
- Maximize IC speed
- Minimize IC power

Opportunities for parallelism

- EDA costumer may use clusters for:
  - simulation: difficult
  - synthesis: difficult
  - place & route: ?
  - mask generation: yes!
- EDA companies use clusters for:
  - unit tests
  - compiling
  - evaluating quality of results

The Synopsys cluster

- 1200 Opteron processors at 2.4-2.8 GHz
- Network: GigEthernet
- OS: Linux
- Main tool: Platform LSF (load sharing facility)
- In November 2006, Synopsys cluster is ranked number 242 in the TOP500 most powerful computer systems in the world

Conclusions

- Parallelism has just started to appear in EDA
- Difficulty: how to parallelize huge programs

References

- SYNOPSYS (htt://www.synopsys.com)
- WORLD OF ASIC (http://www.asic-world.com)
- Platform LSF (http://www.platform.com)