Electronic Design Automation: Evolution, Education, and Profession

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Outline

- Brief Review of Electronics
- How to Design a Chip
- Electronic Design Automation (EDA)
- EDA Education
- EDA Profession
- Summary

Electronic Design Automation

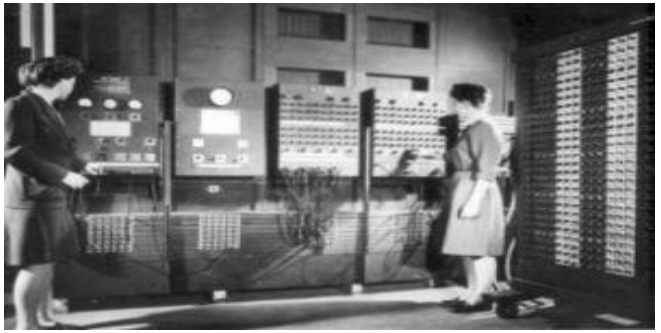
- **Where Electronics Begin**
  - **Electronics (1 trillion market)**
    - **Computer chips, cellular phones, PDA, pacemakers, controls for automobiles and satellites to the servers, routers and switches**
  - **Design**
    - **The part of the production cycle where creativity, new ideas, ingenuity and inspiration are explored.**
  - **Automation**
    - **Techniques and equipment used to achieve automatic operation.**

Scope of Electronics

- **Consumer electronics**
  - **Musicassette (Philips EL 3300 = 1963)**
  - ***Zworykyn*'s iconoscope (1924) and *Farnsworth*'s scanning tube (1927)**
- **Communications**
  - ***Guglielmo Marconi* invented Wireless Telegraphy (1896)**
- **Computers**
  - **Fully functioning electronic computer: ENIAC (1945) at U of Pen.**
- **Defense**
  - **WORLD WAR II**

Philo Farnsworth with his television

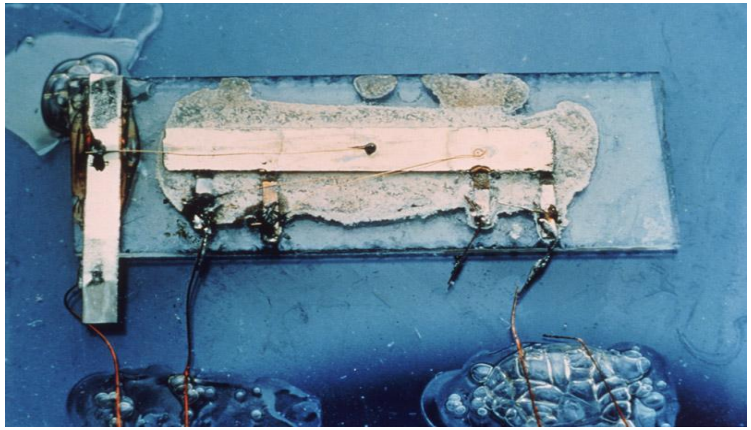
Vladimir Zworykin demonstrates electronic television, 1929



ENIAC's main control panel

Electronic Devices

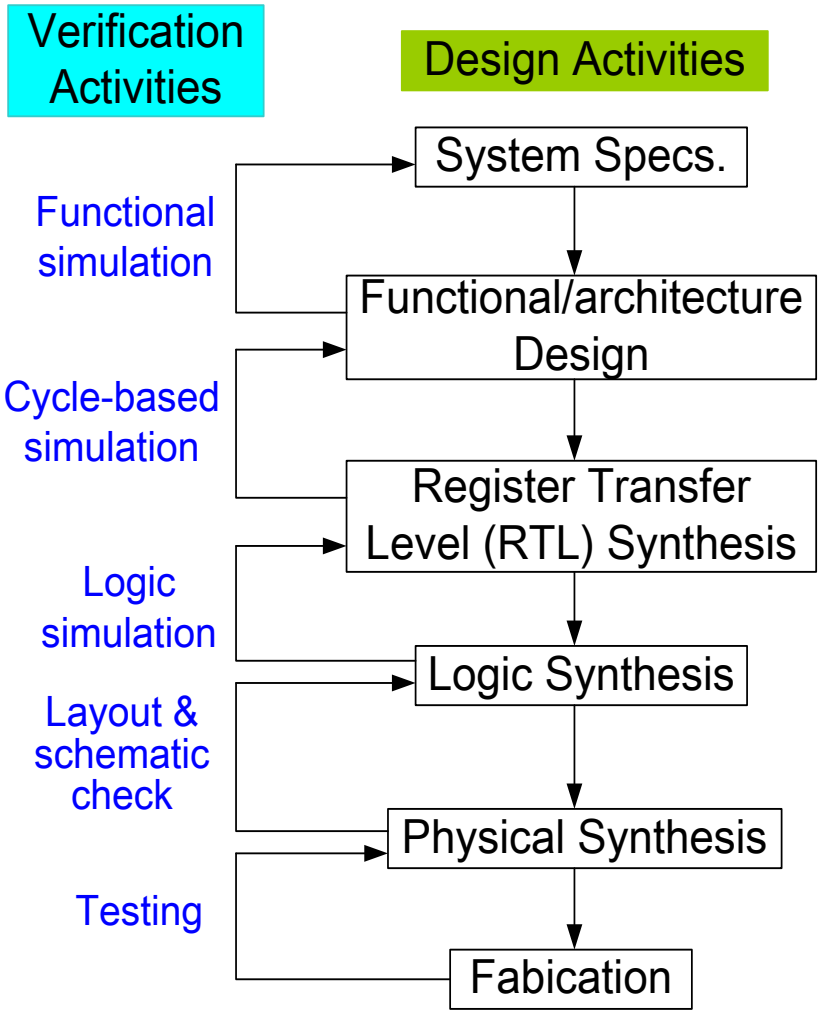
- **Vacuum Tube**
  - ***John Ambrose Fleming***
    - **first electronic rectifier, the diode, or *Fleming Valve* (1904)**
  - ***Lee De Forest***
    - **invention of the audion tube, a three-element vacuum tube (1906)**
- **Transistor**
  - **Discrete**
    - ***John Bardeen, William Shockley*, and *Walter Brattain* at Bell Labs (1947)**
  - **Integrated circuits**
    - ***Jack Kilby* at TI (1959)**
    - ***Robert Noyce* at Fairchild (1959)**



Consequences of Transistor and IC Invention

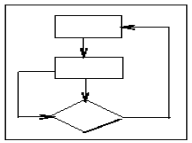
- Open a new era in electronics
- Integration make things smaller and cheaper
- Scaling (transistors going smaller and smaller) enables putting more things in a chip (System-On-Chip)
  - Design problems become increasingly more complex than ever before
- Scaling (Moore's Law) and integration necessitate the help of EDA Tools

How Chips Are Designed?



Design Representations

System C
System Verilog

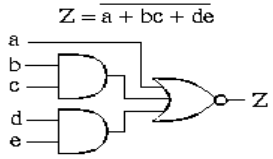


Verilog, VHDL

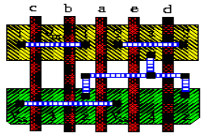
```
always @ (x or a or b or c or d or s)
begin
/*d1*/   x = a + b;
/*d2*/   if ( s ) x = c – d;
/*d3*/   else x = x;
/*d4*/   y = x;
end
```

Verilog, VHDL

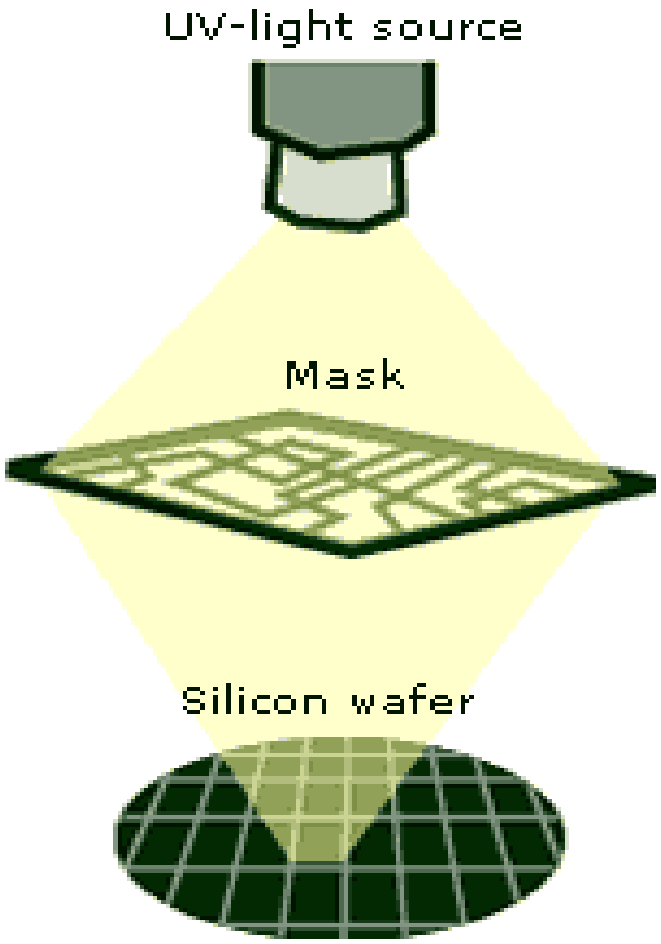
Verilog, VHDL, DEF, EDIF



GDSII



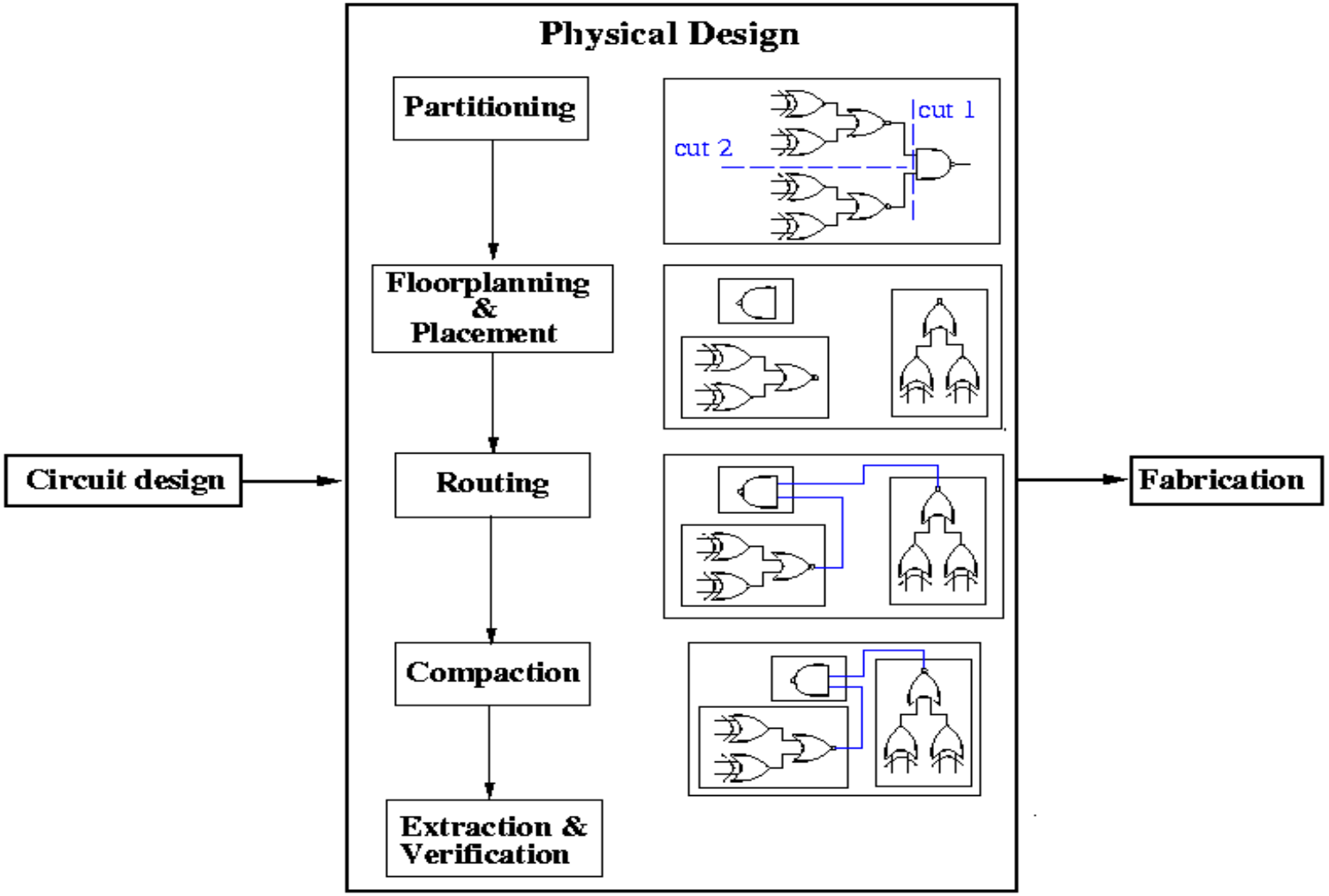
How Chips Are Made?



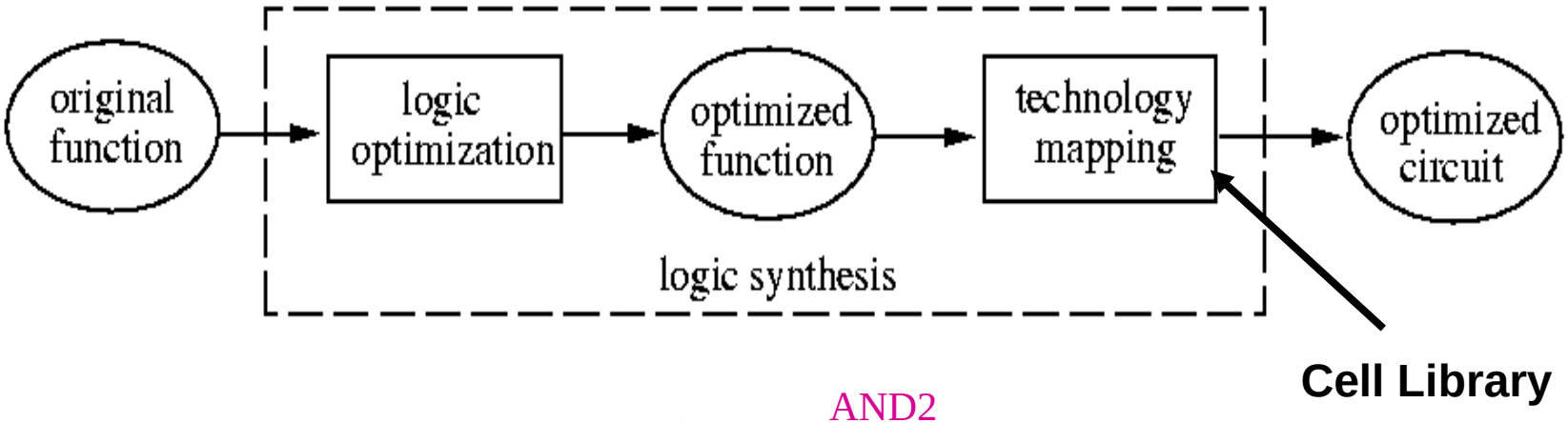
Major Tasks of EDA

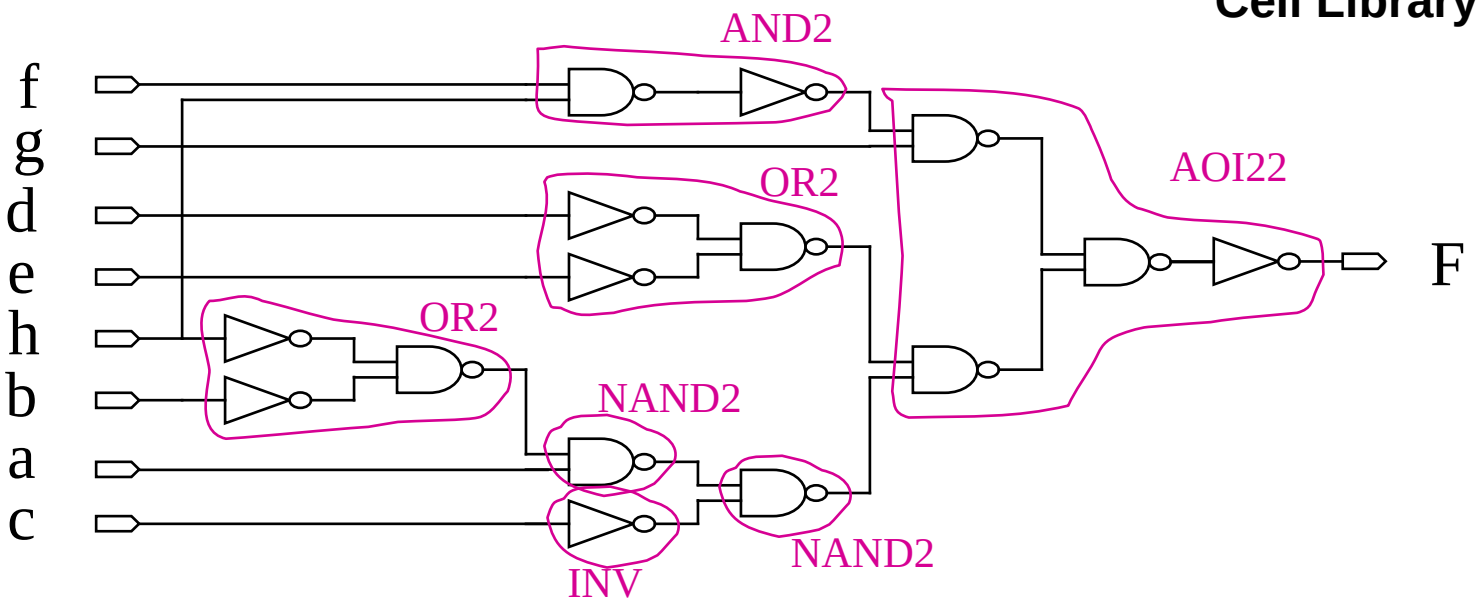
- **Synthesis**
  - **Translation + Optimization**
- **Verification and Simulation**
  - **Verifying the correctness of a design**
- **Analysis**
  - **Knowing how good a design is**
- **Testing**
  - **Knowing whether a chip does work**

Physical Synthesis



Logic Synthesis





RTL Synthesis (1)

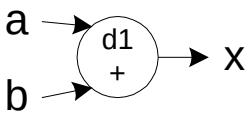
```
always @ (x or a or b or c or d or s)
begin
/*d1*/   x = a + b;
/*d2*/   if ( s ) x = c – d;
/*d3*/   else x = x;
/*d4*/   y = x;
end
```

Input HDL

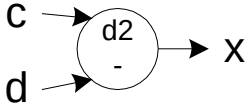
```
always @ (x or a or b or c or d or s)
begin
/*d1*/   x = a + b;
/*d2*/   if ( s ) x = c – d;
/*d3*/   else x = x;
/*d4*/   x = s mux x;
/*d5*/   y = x;
end
```

Modified 3-address code

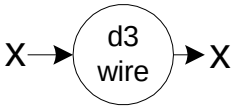
In[d1]={d4, d5}



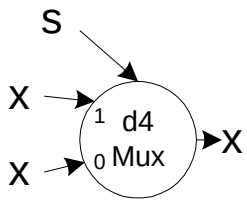
In[d2]={d1, d5}



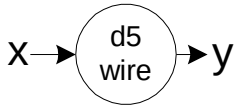
In[d3]={*d1, d5}



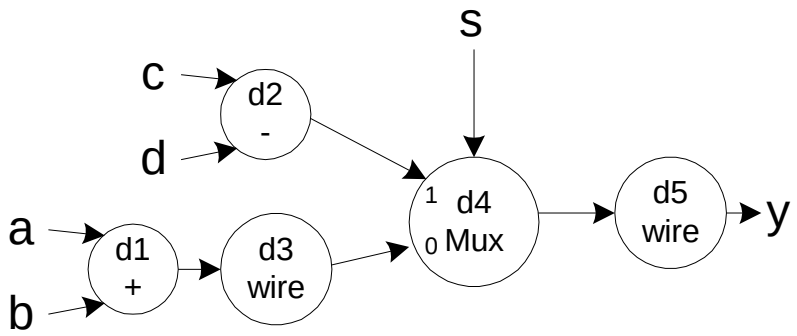
In[d4]={*d2, *d3, d5}



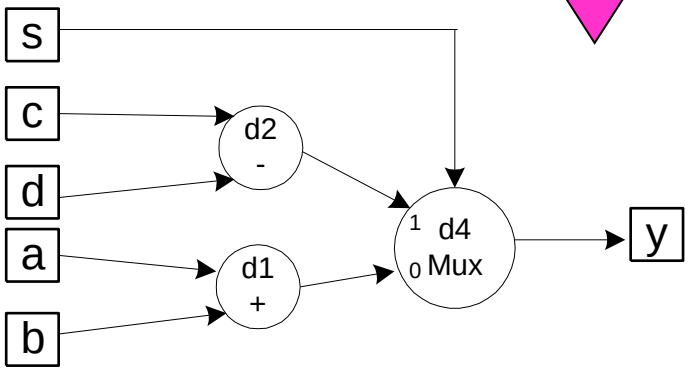
In[d5]={*d4, d5}



computed by control/ data flow analysis



Interconnection binding



Final result

Functional unit allocation

Special Element Inferences

- **Given a HDL code at RTL, three special elements need to be inferred to keep the special semantics**
  - **Latch (D-type) inference**
  - **Flip-Flop (D-type) inference**
  - **Tri-state buffer inference**

```
reg Q;
always@(D or en)
   if(en) Q = D;
```

Latch inferred!!

```
reg Q;
always@(posedge clk)
     Q = D;
```

Flip-flop inferred!!

```
reg Q;
always@(D or en)
   if(en) Q = D;
   else    Q = 1'bz;
```

Tri-state buffer inferred!!

Verification

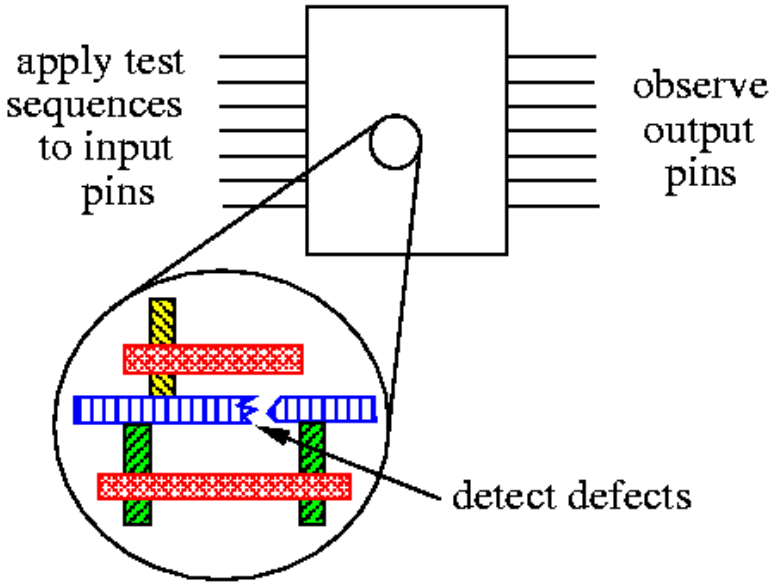
- **To Know whether a design is correctly designed**
  - **Simulation**
  - **Formal Verification**

A ➡ **Translation + Optimization** ➡ **B**

Question: A=B?

Testing

- **To know whether a design is correctly fabricated**
  - **Design for testability**



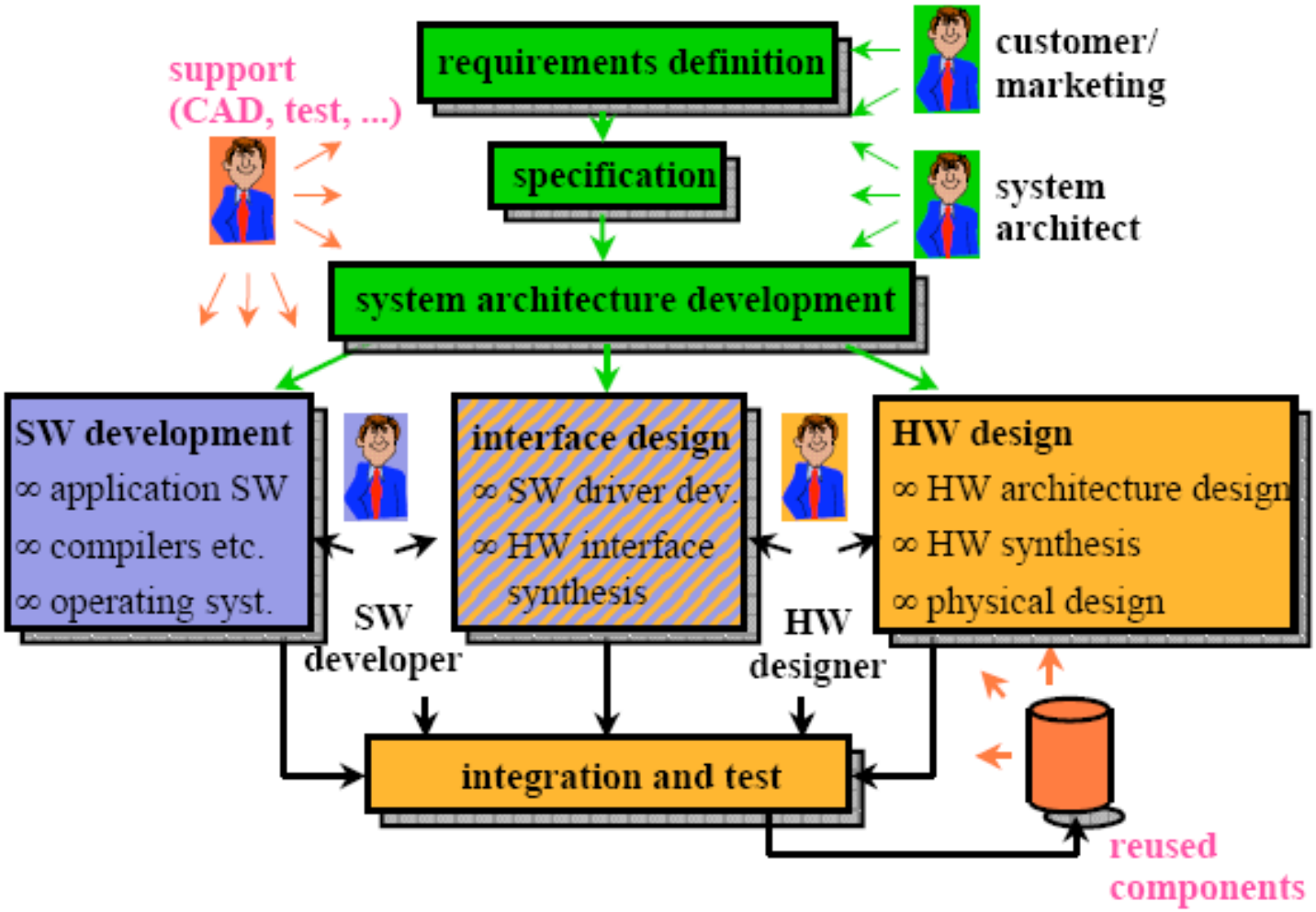
Analysis

- **Timing analysis**
  - **To know how fast a fabricated design can run**
    - **Static timing analysis**
    - **Statistical timing analysis**
    - **Timing simulation**
- **Power analysis**
  - **To know how much energy is consumed**
    - **Dynamic power**
    - **Standby power**

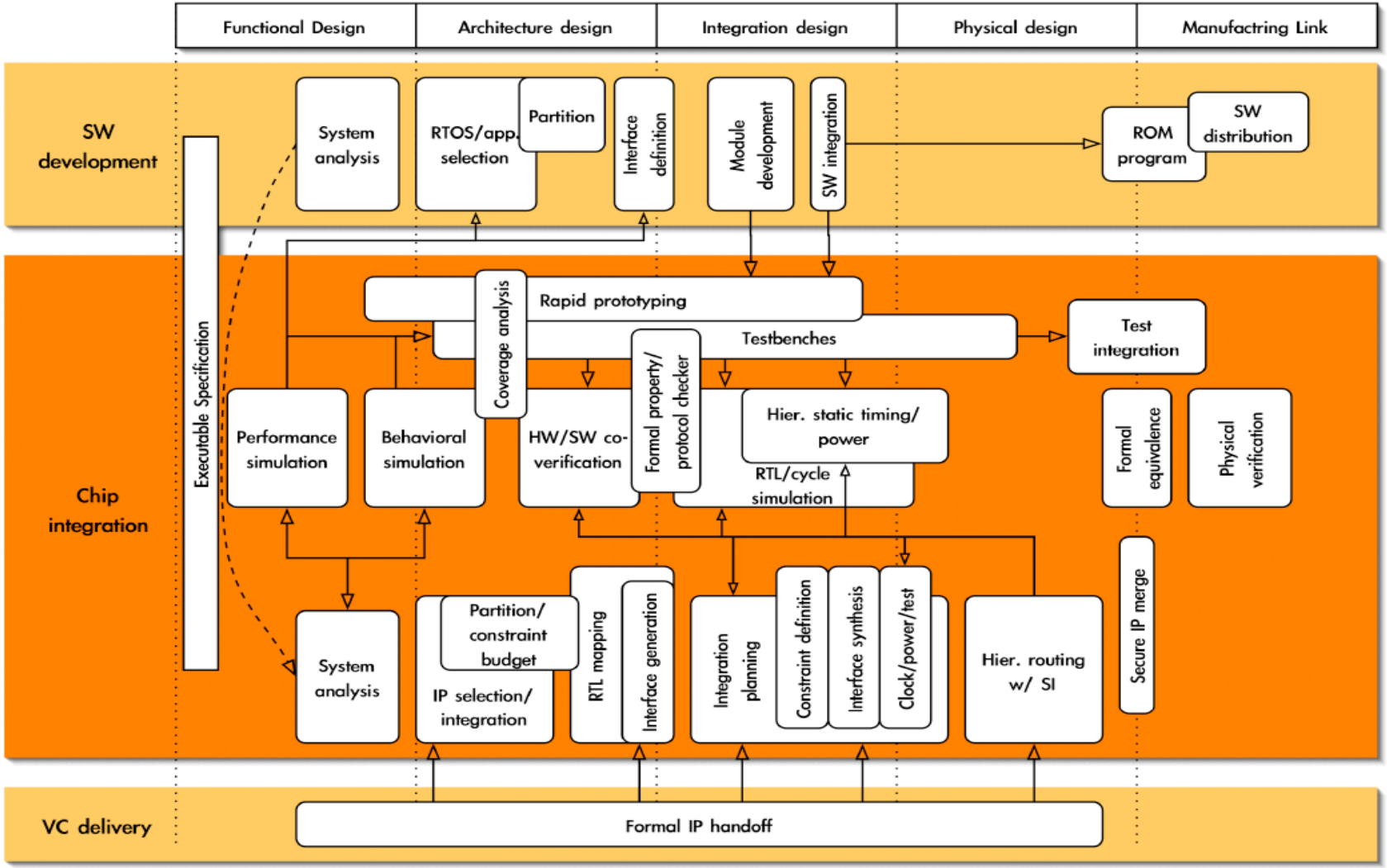
Design Evolution

- Continual increase in complexity
- System-on-Chip (SOC)
- More software and less hardware
- More applications oriented
  - Embedded system designs
- Coping with design problems associated with process technology

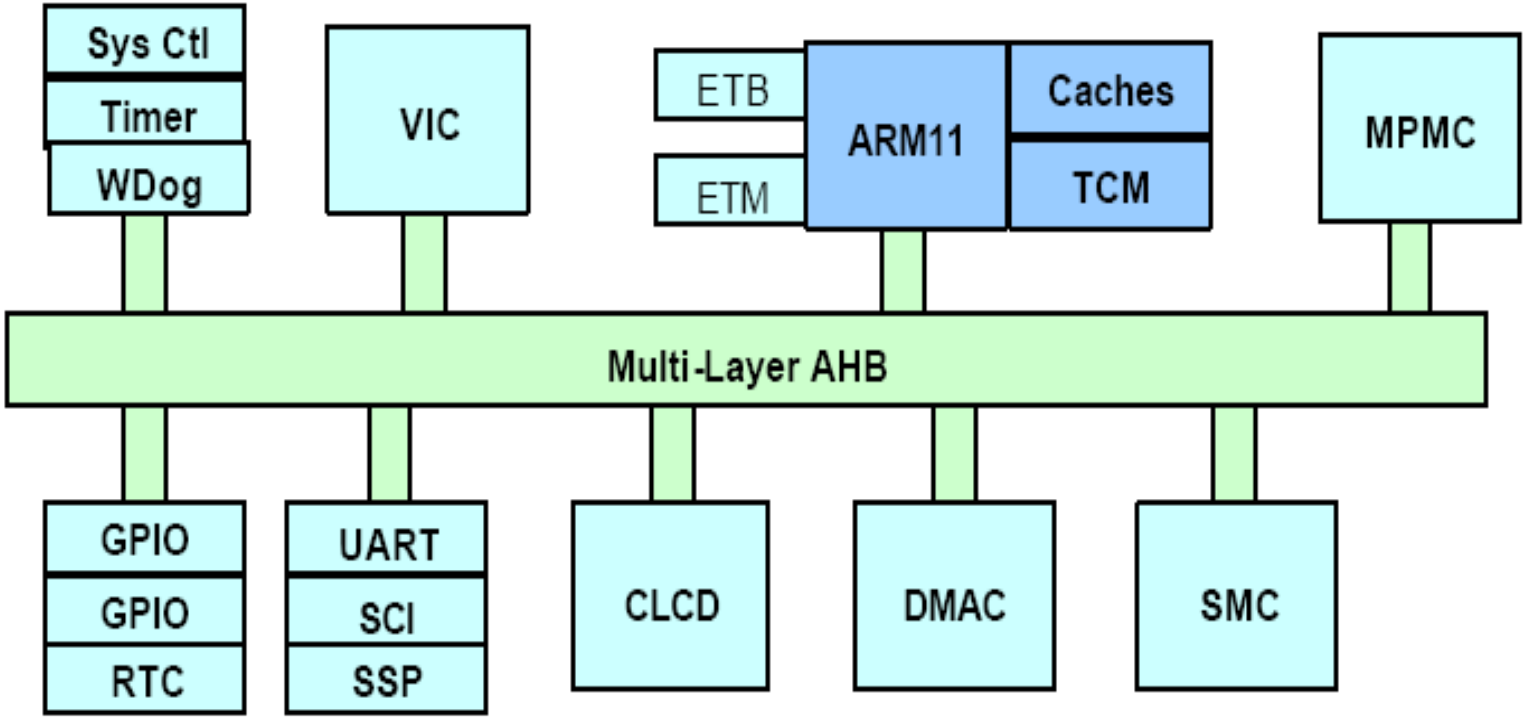
Embedded System Design



Platform-Based Design (PBD) for Coping Complexity



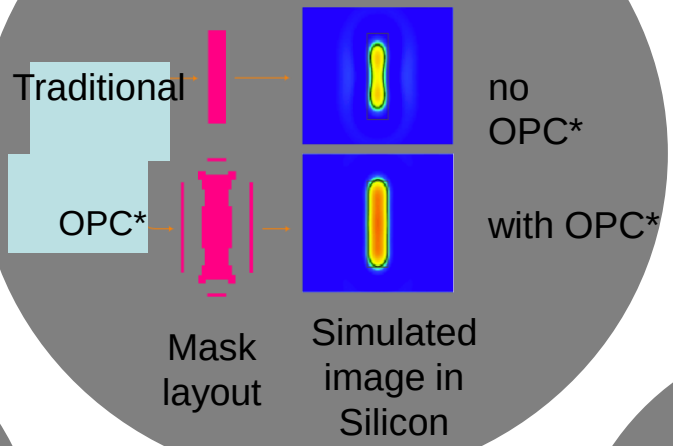
An Example of Platform Architecture



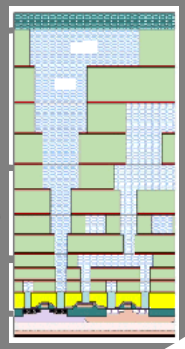
Design Problems with Process Technology

*OPC = Optical Proximity Correction

Lithography



Design Complexity



Materials

Dishing during Copper CMP

EDA: How was it started?

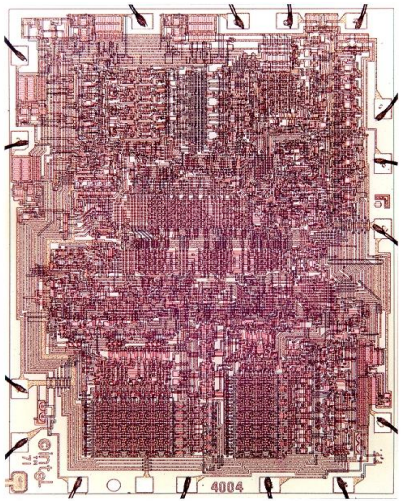
- **Also called Computer-Aided Design (CAD)**
  - **It was started from automating drawing systems that helped create the drawings of boards and systems.**
  - **Around 1969, IC mask maker and flatbed plotter invented.**

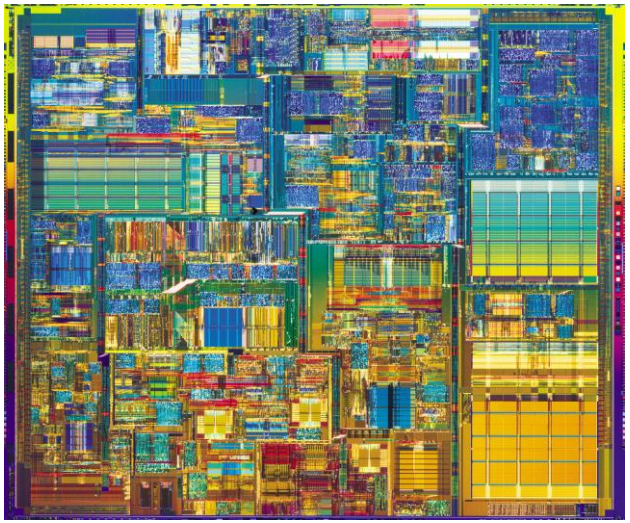
How EDA Evolves?

- **In the beginning**
  - **To avoid errors**
- **Later**
  - **To increase performance and reduce production cost**
- **Now**
  - **To increase productivity, reduce design cost, and reduce Time-to-Market**

Evolution of Computers

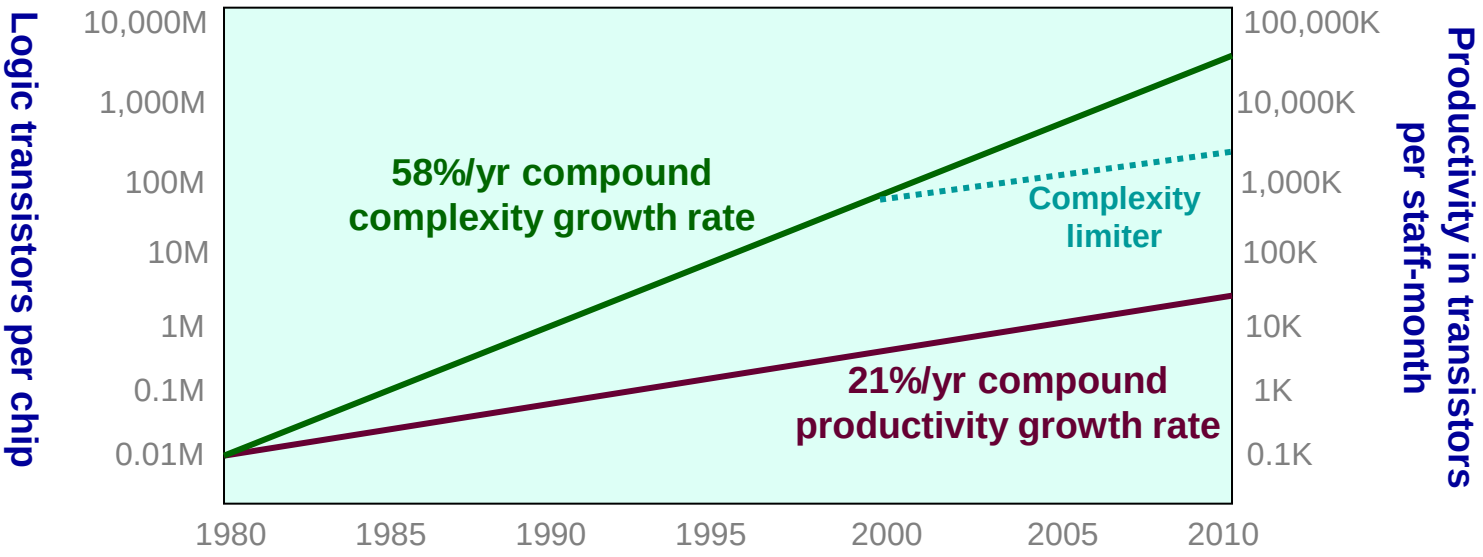
- **ENIAC (1945)**
  - **Fully functioning electronic computer**
- **UNIVAC-1 (1951)**
  - **First commercially successful electronic computer**
- **Second Generation Computers (1959)**
  - **Transistors built**
- **Intel 4004 (1971)**
  - **First microprocessor**
- **Intel P4 (2003)**
  - **42 millions transistors**



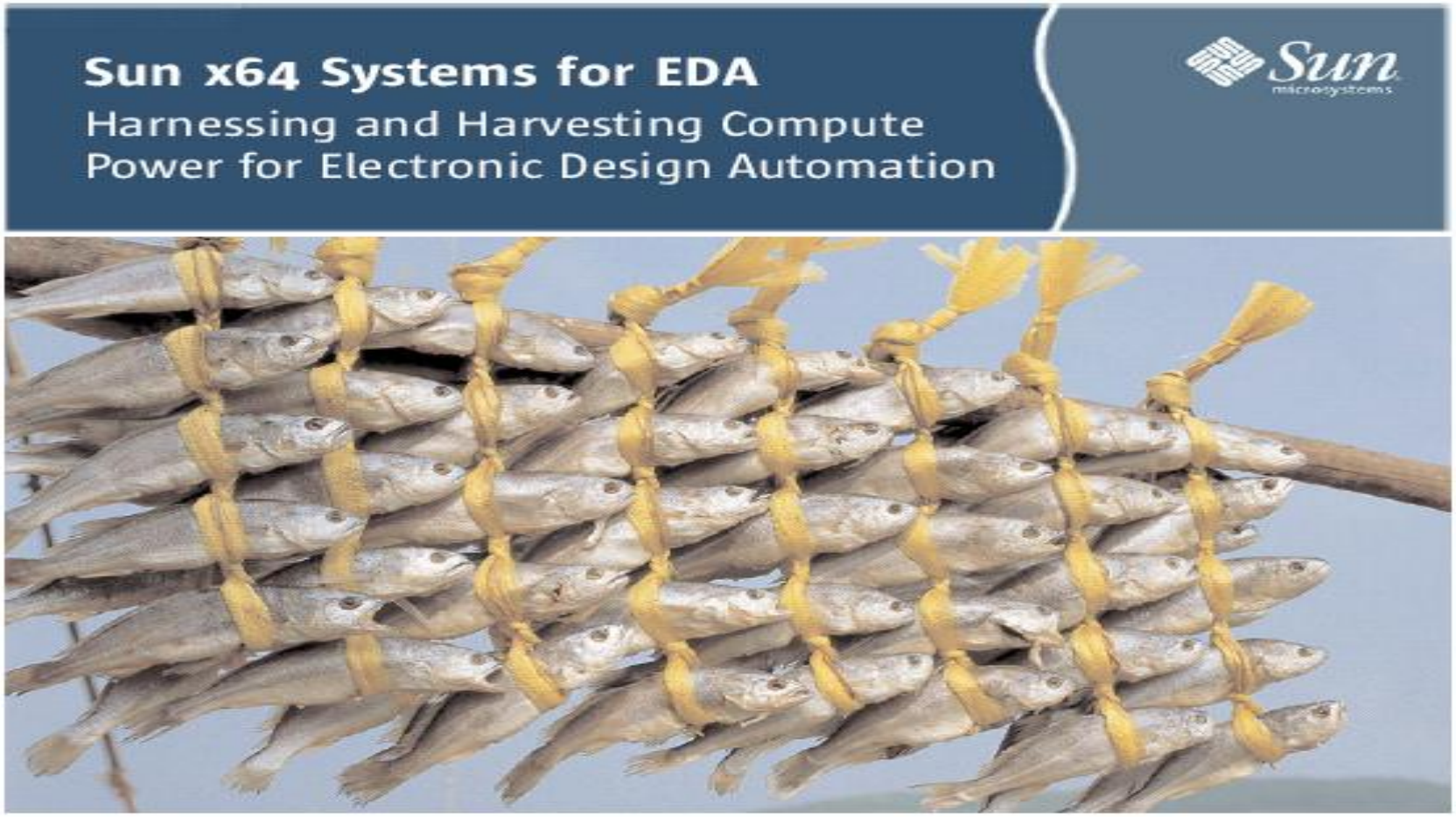


Co-Evolution of EDA

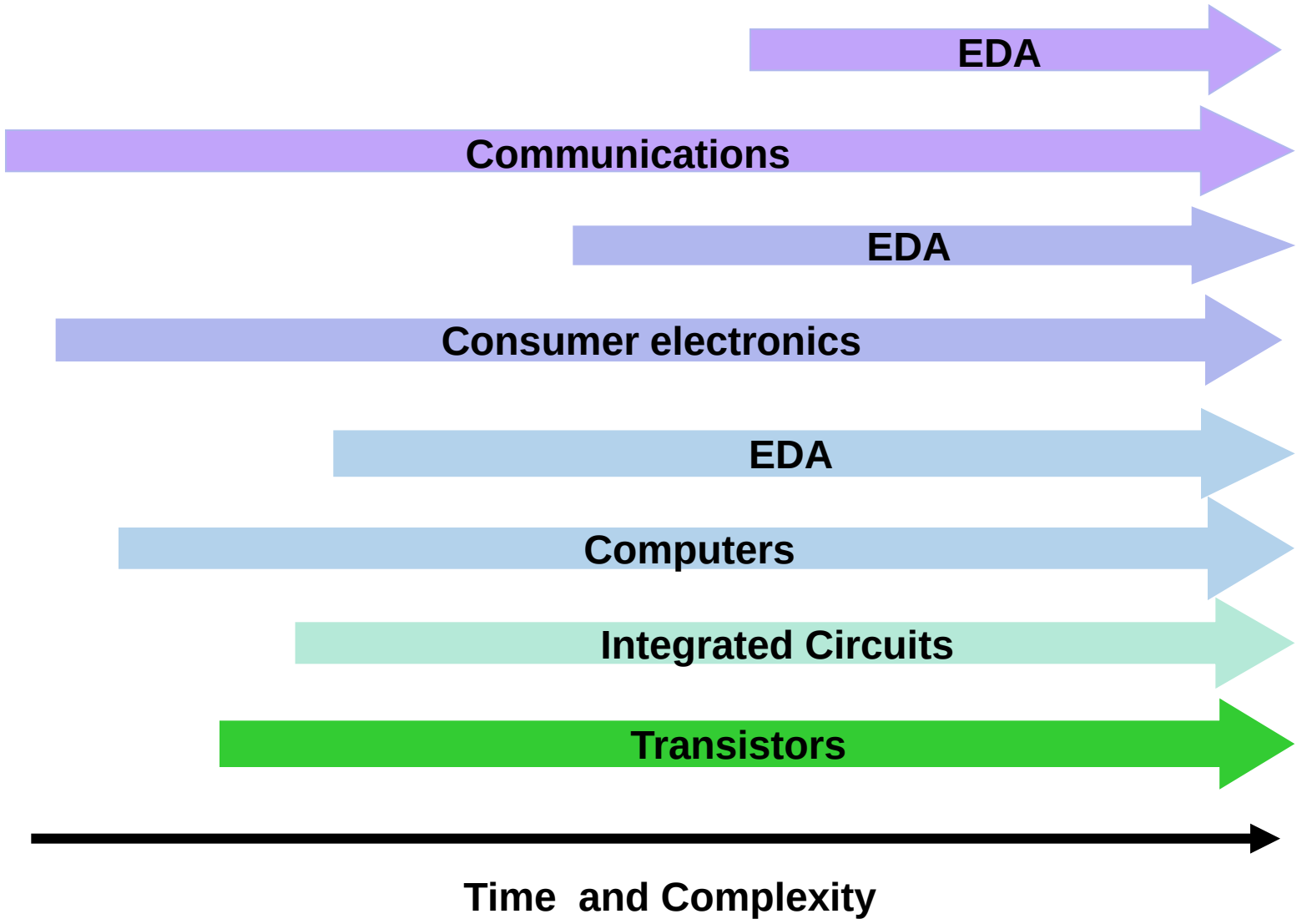
- **With computer designs and process technology**
  - **Moore's Law: Transistor density doubled every 18 months**
  - **Intractable complexity of making more powerful computing machines**
  - **Use of EDA to cope with complexity and increase productivity**



EDA and Fish?


Sun x64 Systems for EDA
Harnessing and Harvesting Compute Power for Electronic Design Automation
Sun
microsystems

Tides of EDA


EDA
Communications
EDA
Consumer electronics
EDA
Computers
Integrated Circuits
Transistors
Time and Complexity

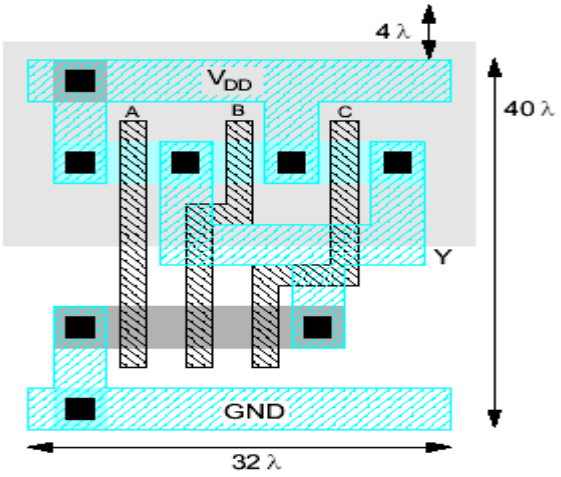
Eden of EDA: Silicon Compilation

- **Software design**
  - **Design description using high level lang.**
  - **Compilers translate the description into instructions**
- **Hardware design**
  - **Design description using HDL**
  - **Design compilers translate the description into logic gates**
  - **Physical compilers translate logic gates into transistor implementation**

Why Silicon Compilation Fails?

- **Failing at using physical compilers to translate logic gates into transistor implementation**
  - **Performance**
  - **Power**
  - **Area**
  - **Signal integrity**

Governed by the evolution of semiconductor process technology

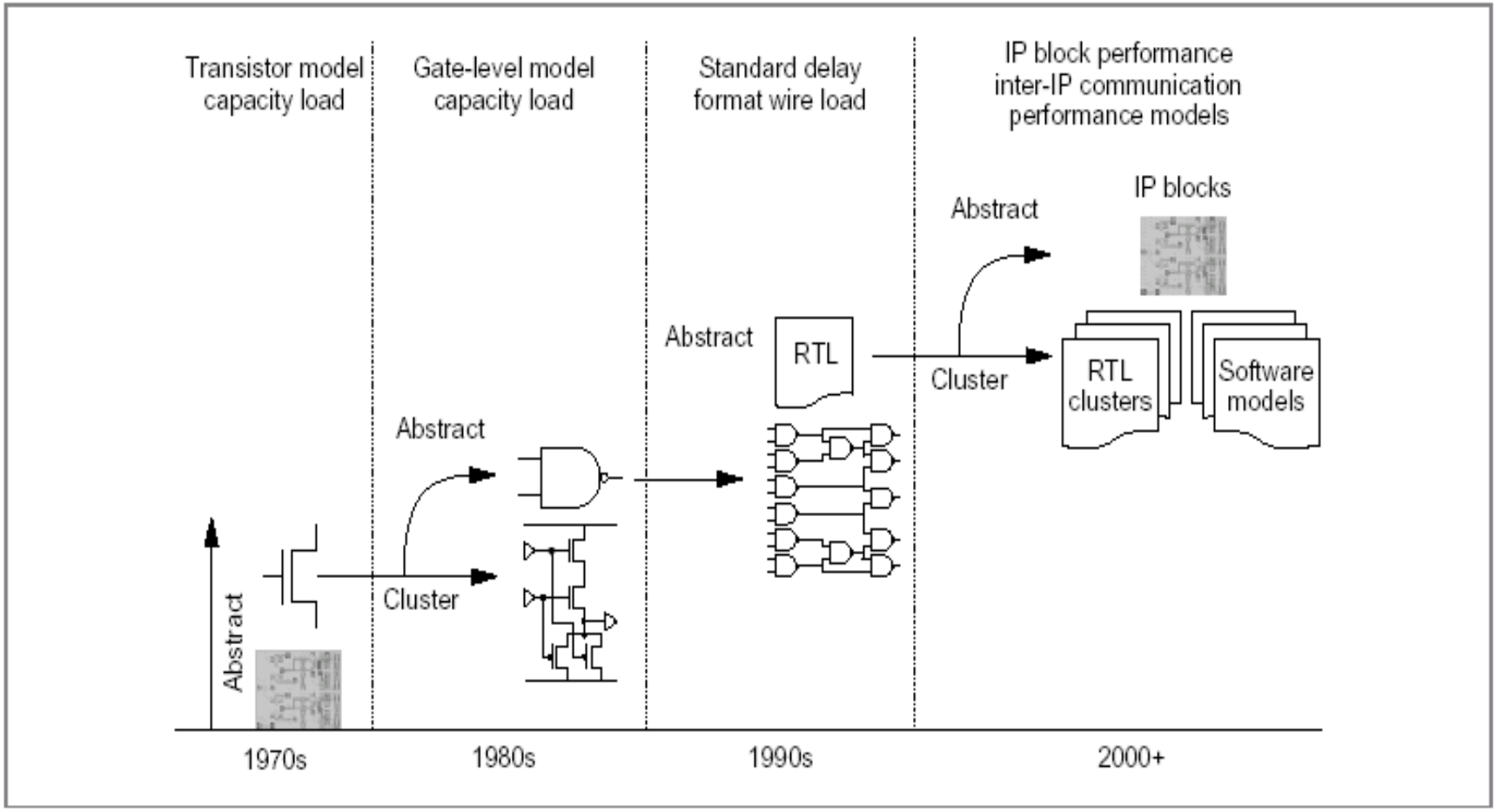


Difficult to optimize every aspect of a design and achieve the trade-off set by designer's intent

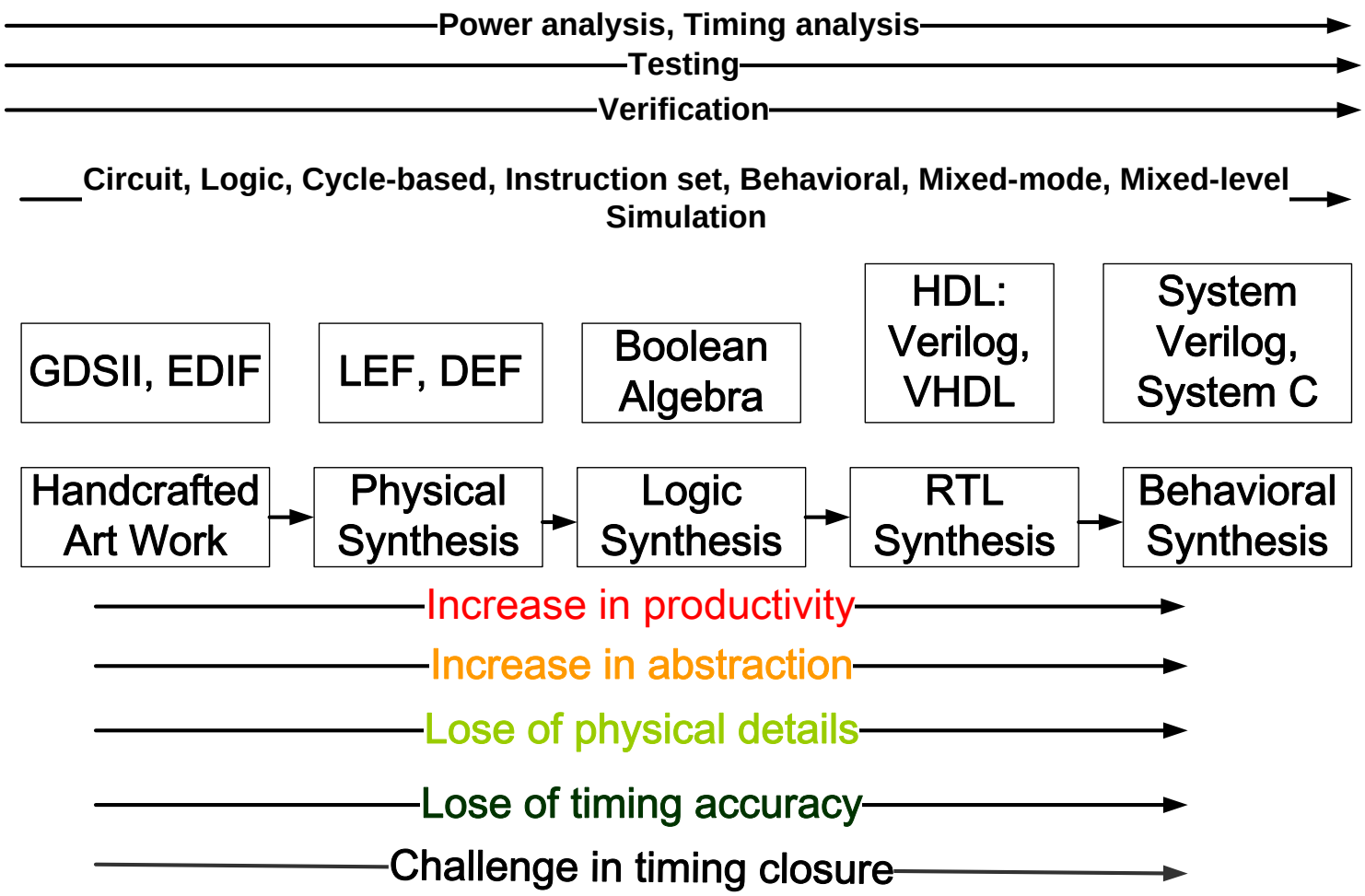
Where Is EDA Going?

- Raising abstraction level for performing design space exploration and simplifying design verification
- Lowering the implementation level to optimize power, delay, and area
  - Leakage problem
  - Process variation
    - Manufacturing aspect
    - Timing aspect

Raising Abstraction Level

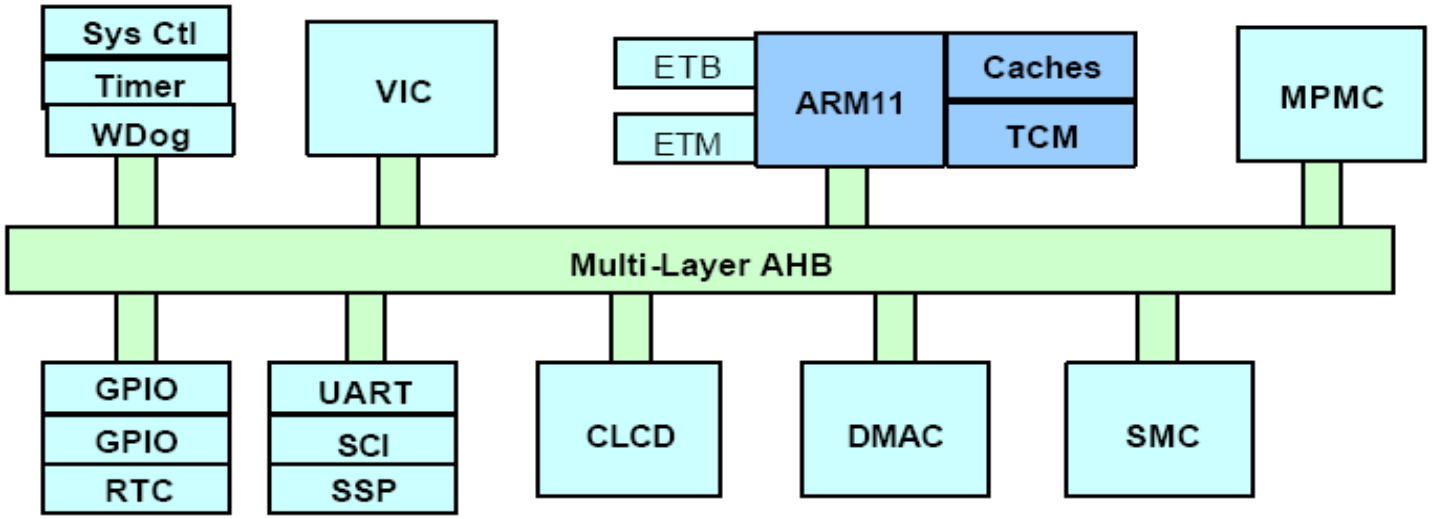


Increase in Productivity



Enabling EDA to Support PBD

- IP creation and validation
- IP integration
- System level synthesis and verification
- Hardware and software design space exploration
- Taking advantage of process advancement

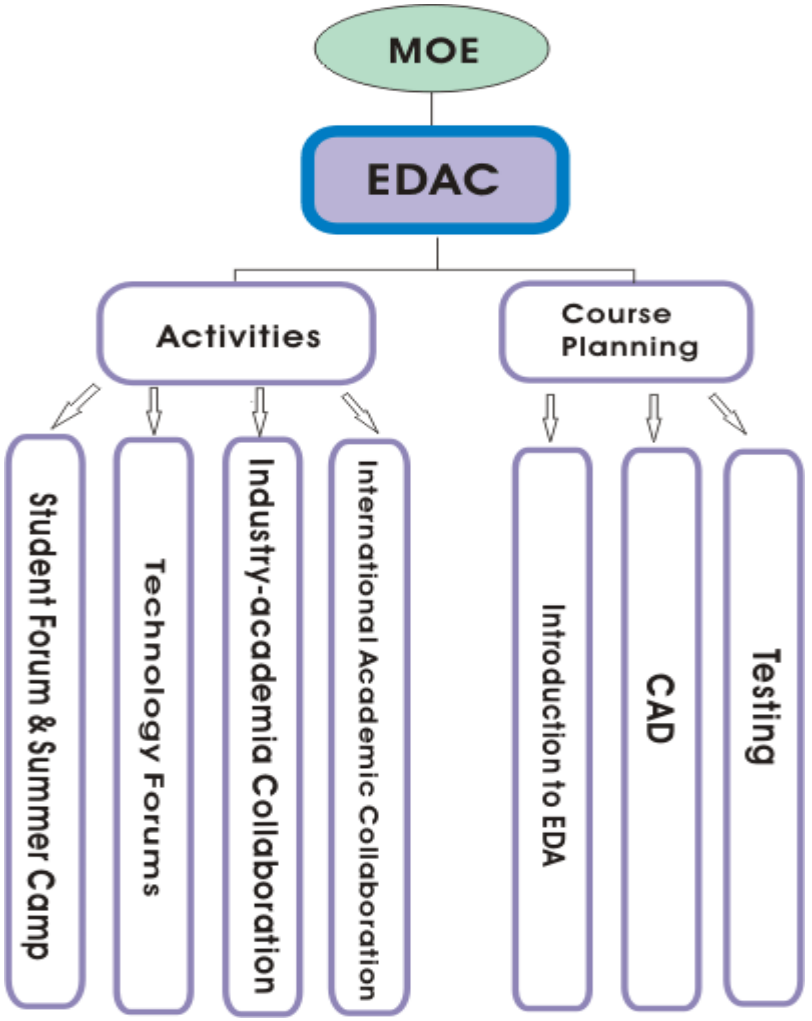


EDA Education

- **An interdisciplinary training**
  - **Data structure, algorithm, discrete math, programming, digital system design, VLSI design, electronics, circuit theory, etc**
- **Not really having an EDA program**
  - **Not even having a good textbook for it**
  - **Traditionally, one or two courses in Computer Science or Electrical Engineering**

EDA Education in TAIWAN

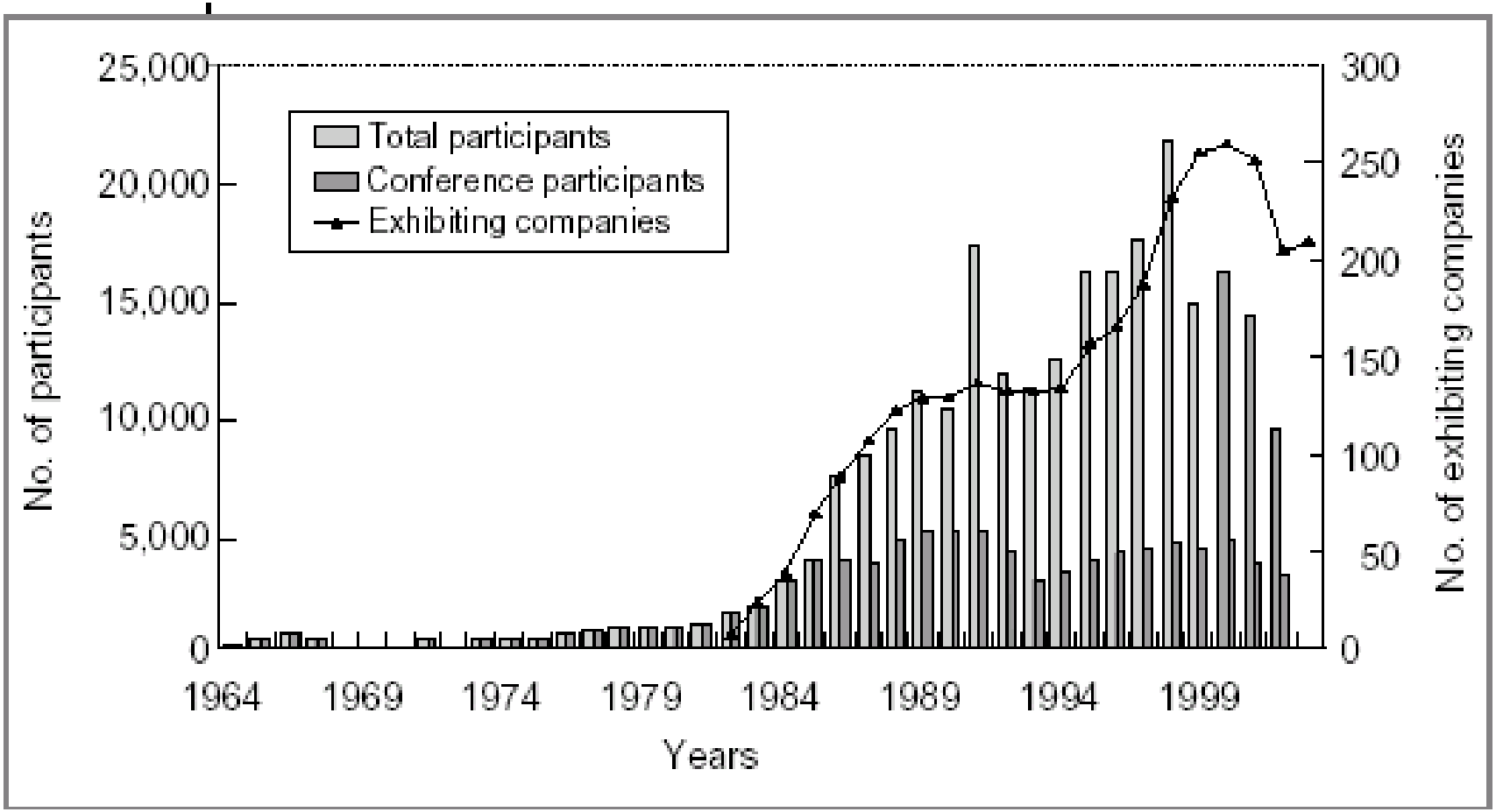
- **Electronic Design Automation and Test (DAT) Consortium**
  - **founded in 2002 under Ministry of Education, Taiwan**



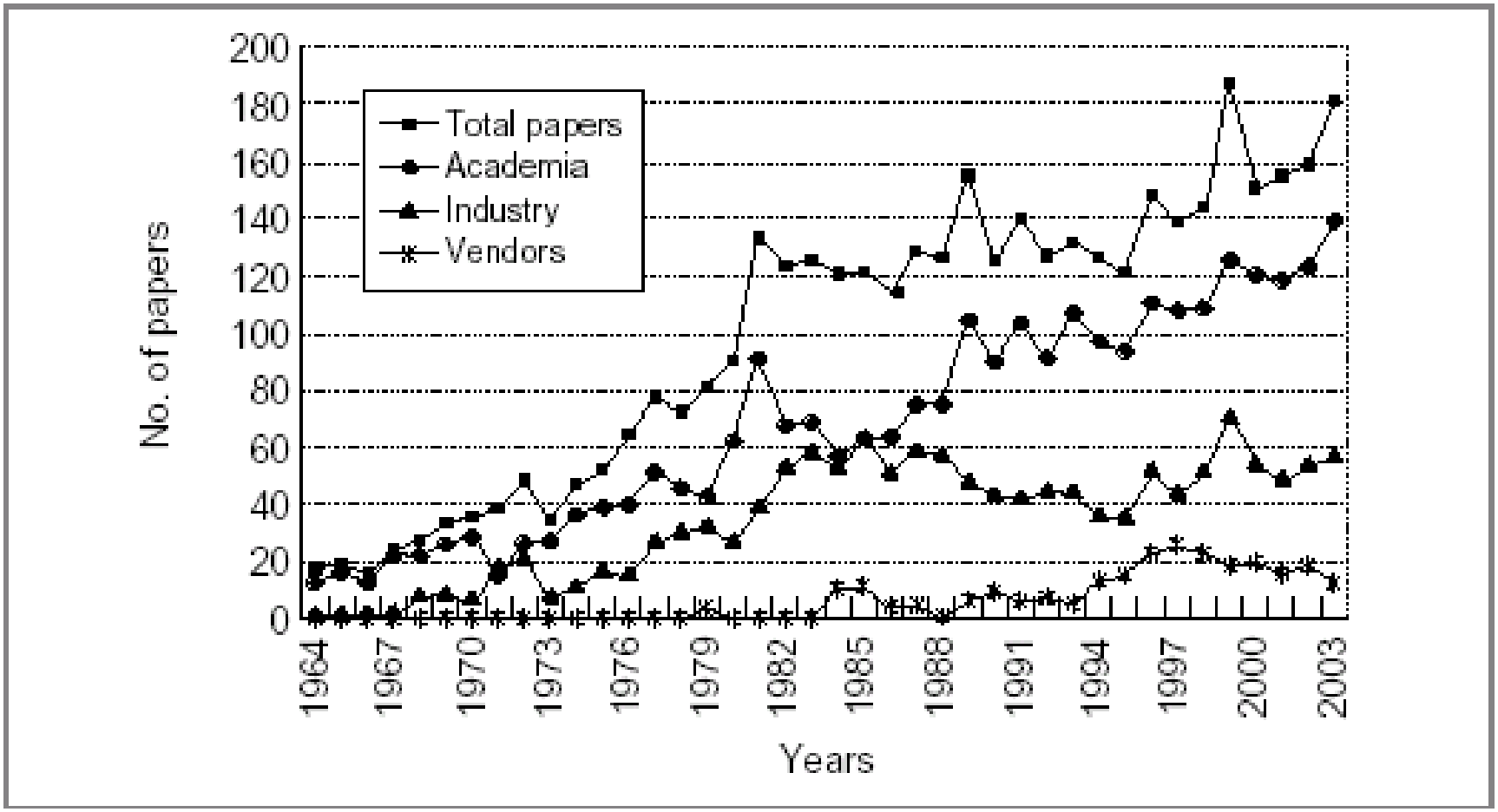
EDA Conferences

- **Design Automation Conference (DAC)**
  - **Started in 1964**
- **International Conference on CAD (ICCAD)**
  - **Started in 1982**
- **International Conference on Design, Automation and Test in Europe (DATE)**
  - **Started in 1998**
- **ASPDAC, VLSI-DAT, ISQED, ISPD, …**

DAC Statistics: Attendance



DAC Statistics: Papers



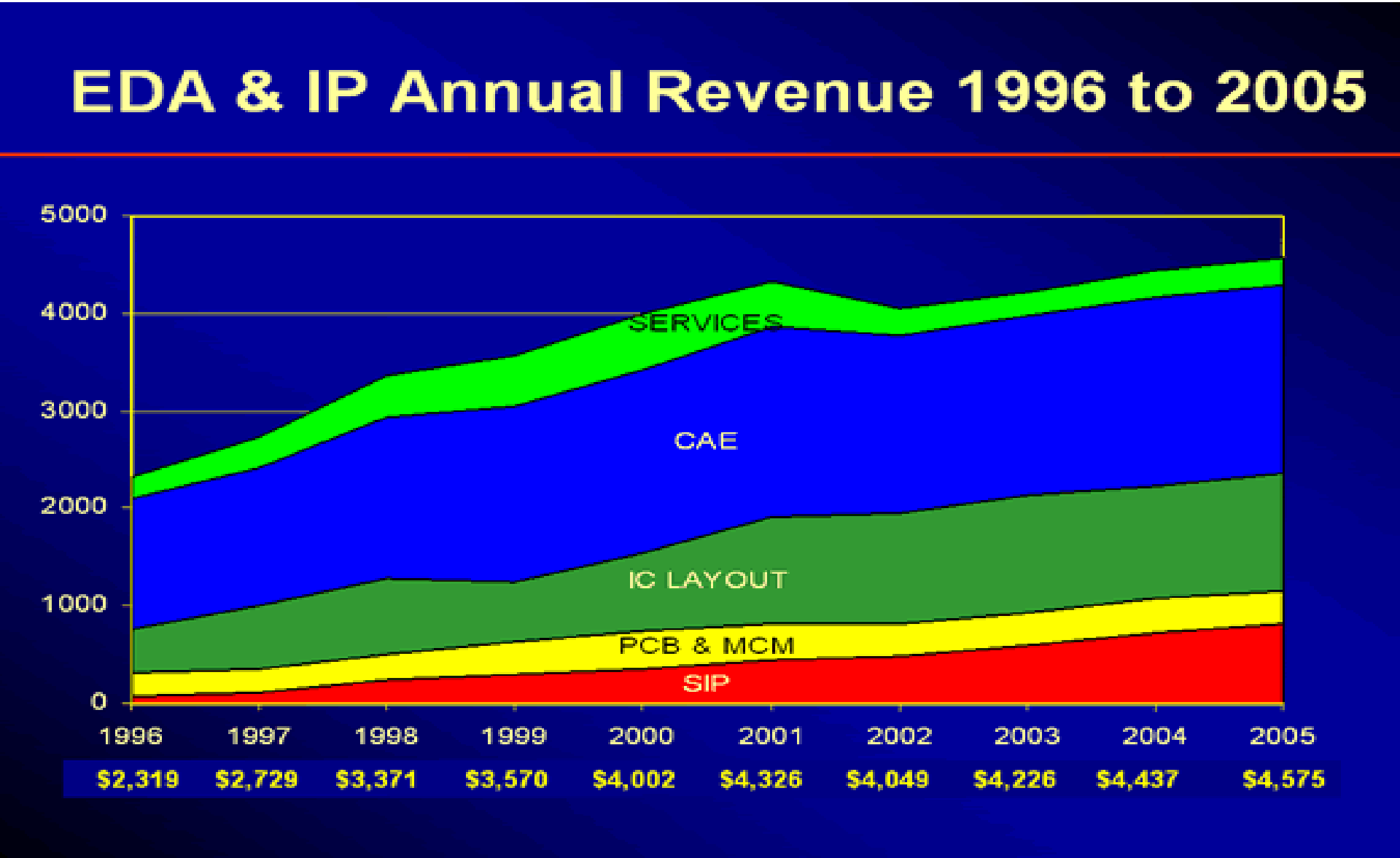
EDA Business

- A rich history of invention and innovation
- A history of merging
- Business evolution
  - Hardware
  - Hardware + software
  - Software only

Main EDA Players

- **Cadence**
- **Synopsys**
- **Mentor Graphics**
- **Magma**
- **Springsoft**
- **PDF solutions**

Market Value



Work on EDA?

- **EDA employs over 20,000 people and more than 500,000 people use its tools and services.**
- **Highly rewarding and challenging**

Career in EDA

- **EDA companies**
- **IC design houses**
- **IC design service companies**
- **Semiconductor foundries**
- **Integrated, design, and manufacturing (IDM) companies**
- **Consultants**

Who Can Work on It?

- **One is smart, hard working, communicable, and likes it.**
  - **Integrity**
- **One knows hardware and software**
- **One better has a master degree**
- **One knows “Who controls the past commands the future. Who commands the future conquers the past.”**

EDA Infrastructure Software Engineer in CA-Cupertino

- **Company: CyberCoders**
- **Base Pay: $100,000.00 - $110,000.00 /Year**
- **Relocation: Yes**
- **Experience: More than 5 Years**
- **Employee Type: Full-Time**
- **Employee Education: 4 Year Degree**
- **Contact Name: Sandy Messerli Phone: 949-8855138**
- **EDA Infrastructure Software Engineer**
  - **Required Skills: EDA infrastructure, EDA, design database, OpenAccess, Java, XML, electronic design automation**

EDA Engineer at TSMC

- **IC設計類 - Design Flow Development and Application Manager/Engineer**
  - **Master degree in Electrical Engineering, Computer Science/Engineering, or related engineering fields**
  - **Minimum 3 years of experience in chip implementation, design flow, or electronic design automation (EDA).**
  - **Technical expertise in one of the following areas are preferred: VLSI technologies, IC design flow, design for manufacturability (DFM)**
  - **Experienced in commercial EDA tools (e.g., Synopsys, Cadence, Mentor, Magma etc)**
  - **Ability to conduct technical meetings, presentations, and training to customers is preferred**

IC Design Manager at TSMC

- **IC設計類 - Manager - CAE 碩士/博士畢業、電子相關科系/電機相關科系/資訊工程相關、8 年以上工作經驗**
  - **Minimum master degree in Electronics Engineering or Computer Science.**
  - **Minimum 8 years experience in IC/IP design and EDA tools.**
  - **Strong communication and project management skills**
  - **Fluent in English.**
  - **Work location in Hsinchu, Taiwan**

Summary

- **EDA where electronics begin**
  - **A good command at EDA will increase design productivity and shorten time-to-market of a product.**
- **Career in EDA is challenging and rewarding**

Thank You Very Much